

Substitute for Form 1449/PTO

Complete if Known

INFORMATION DISCLOSURE

STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet

1

of

2

Attorney Docket Number

P16015C

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)				
V-Y		us-	5,963,810	10/5/1999	Gardner et al.	_____
✓Y		us-	6,027,976	2/22/2000	Gardner et al.	_____
✓Y		us-	2002/0197790 A1	12/26/2002	Kizilyalli et al.	_____
✓Y		us-	2003/0045080 A1	3/6/2003	Visokay et al.	_____
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ³
		Country Code ⁴	Number ⁴ Kind Code ⁵ (if known)				
V-Y		EP	0 641 027 A	10/5/1999	Ohmi Tadahiro	_____	

Examiner
Signature

V. Y. Gardner

Date Considered

01/04/05

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Substitute for Form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
				Application Number	10/748,090
				Filing Date	December 29, 2003
				First Named Inventor:	Justin K. Brask et al.
				Art Unit	Unknown 2825
Examiner Name	Unknown V. Yezhikov				
Sheet	2	of	2	Attorney Docket Number	P16015C
NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published			T ²
VY		Chih-Wei, Yang et al, "Dramatic Reduction of Gate Leakage Current in 1.61nm HfO2 High-K Dielectric Poly-silicon Gate with A1203 Capping Layers", Electronics Letters, Vol. 38, NO. 20, September 2002, pages 1223-1225, XP002288765			
VY		Osten, H.J. et al., "Epitaxial, High-K Dielectrics on Silicon: The Example of Praseodymium Oxide", Microelectronics and Reliability, Elsevier Science Ltd, GB, Vol. 41, 2001, pages 991-994 XP002265638			
VY		PCT International Search Report PCT/US 03/40688			

Examiner Signature	V. Yezhikov	Date Considered	01/04/05
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				Application Number	Not yet assigned
				Filing Date	Herewith
				First Named Inventor:	Justin K. Brask et al.
				Art Unit	Not yet assigned 142 28 25
				Examiner Name	Not yet assigned V. Yeaslick
				Attorney Docket Number	P16015C

U.S. PATENT DOCUMENTS						
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		Number-Kind Code ² (if known)				
VY ↑ ↓ VY		US-	2002/0197790 A1	12/26/2002	Kizilyalli et al.	_____
		US-	6,514,828 B2	2/4/2003	Ahn et al.	_____
		US-	6,436,777 B1	8/20/2002	Ota	_____
		US-	2003/0045080 A1	3/6/2003	Visokay et al.	_____
		US-	6,544,906 B2	4/8/2003	Rotondaro et al.	_____
		US-	6,184,072 B1	2/6/2001	Kaushik et al.	_____
		US-	6,420,279 B1	7/16/2002	Ono et al.	_____
		US-	2003/0032303 A1	2/13/2003	Yu et al.	_____
		US-	5,783,478	7/21/1998	Chau et al.	_____
		US-	6,625,217	4/29/1997	Chau et al.	_____
	US-	6,306,742 B1	10/23/2001	Doyle et al.	_____	
	US-	5,891,798	4/6/1999	Doyle et al.	_____	
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		Country Code ³	Number ⁴ Kind Code ⁵ (if known)				

Examiner Signature	V. Yeaslick	Date Considered	01/09/05
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VY		Doug Barlage et la. "High Frequency Responset of 100nm Integrated CMOS Transistors with High-K Gate Dielectrics", 2001 IEEE, 4 pages			
VY		ROBERT S. CHAU ET AL. "A 50NM Depleted-Substrate CMOS Transistor (DST)", 2001 IEEE, 4 pages			
VY		"A Method of Making a Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/082,530, filed 2/22/02			
VY		"A Method of Making a Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/285,915, Filed 10/31/02			
VY		"A Method of Making a Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/288,043, Filed 11/5/02			
VY		"A Method of Making a Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/315,268, Filed 12/10/02			
VY		"A Method of Making a Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/338,174, Filed 1/7/03			
VY		"A Method of Making a Semiconductor Device Having a High-K Gate Dielectric", Serial No. Unknown, Filed 3/11/03			

Examiner Signature	V. Yerusha	Date Considered	01/04/05
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